PATENT APPLICATION
DOCKET NO.: 200311777-1

LISTING OF THE CLAIMS

Pursuant to 37 C.F.R. §1.121, provided below is a listing of the pending claims.

1. (Currently Amended) A method for enabling a first circuit analysis tool to flatten a hierarchical design for processing by a second circuit analysis tool, the method comprising:

reading a logical representation of the hierarchical design; [[and]]

identifying a particular block of the hierarchical design to be flattened into a flat representation of the particular block;

loading RC information for the particular block from an RC model of the hierarchical design, the particular block including any instantiations of child blocks at a level lower than the particular block's level; and

writing a flat representation of the particular block to a file available to the second circuit analysis tool, wherein the instantiations of the child blocks may be rotated with respect to one another.

~~for each block of the hierarchical design:~~

~~loading RC information for the block from an RC model of the hierarchical design; and~~

~~writing a flat representation of each instantiation of the block to the second circuit analysis tool.~~

2. (Currently Amended) The method of claim 1 further comprising deleting the RC information for the particular block from the RC model.

3. (Original) The method of claim 1 further comprising flattening all blocks in a first hierarchical level of the hierarchical design before flatting a block in a next hierarchical level of the hierarchical design.

4. (Original) The method of claim 1 further comprising flattening all blocks of a net of the hierarchical design before flattening a block of another net of the hierarchical design.

5. (Original) The method of claim 4 wherein at least one of the blocks of the net is in a different hierarchical level than at least one other one of the blocks of the net.

6. (Original) The method of claim 1 wherein a storage capacity of the second circuit analysis tool is greater than a storage capacity of the first circuit analysis tool.

7. (Currently Amended) A method for enabling a first circuit analysis tool to flatten a hierarchical design for processing by a second circuit analysis tool, the method comprising:

reading an RC representation of the entire hierarchical design; [[and]]

identifying a particular block of the hierarchical design to be flattened into a flat representation of the particular block, wherein the particular block is operable to include instantiations of child blocks at a level lower than the particular block's level; and

writing a flat representation of the particular block to an external file available to the second circuit analysis tool, wherein the instantiations of the child blocks may be rotated with respect to one another.

~~for each block of the hierarchical design, writing a flat representation of the block to an external file.~~

8. (Original) The method of claim 7 further comprising, responsive to flattening of all blocks comprising the hierarchical design, saving the external file.

9. (Currently Amended) The method of claim 8 wherein the external file is saved to a memory accessible to [[of]] the second circuit analysis tool.

10. (Original) The method of claim 7 further comprising, responsive to flattening of all blocks comprising the hierarchical design, the second circuit analysis tool processing the external file.

11. (Original) The method of claim 7 wherein a storage capacity of the second circuit analysis tool is greater than a storage capacity of the first circuit analysis tool.

12. (Currently Amended) A system for flattening a hierarchical design to be processed by an external circuit analysis tool, the system comprising:

means for reading a logical representation of the hierarchical design;

means for identifying a particular block of the hierarchical design to be flattened into a flat representation of the particular block;

means for loading RC information for [[a]] the particular block of the hierarchical design from an RC model of the hierarchical design, the particular block including any instantiations of child blocks at a level lower than the particular block's level; and

means for writing a flat representation of the particular block to a file available ~~each instantiation of the block~~ to the external ~~second~~ circuit analysis tool, wherein the instantiations of the child blocks may be rotated with respect to one another.

13. (Currently Amended) The system of claim 12 further comprising means for deleting the RC information for the particular block from the RC model subsequent to the flattening.

14. (Original) The system of claim 12 wherein all blocks in a first hierarchical level of the hierarchical design are flattened before any blocks in a next hierarchical level of the hierarchical design are flattened.

15. (Original) The system of claim 12 wherein all blocks of a net of the hierarchical design are flattened before any blocks of another net of the hierarchical design are flattened.

16. (Original) The system of claim 15 wherein at least one of the blocks of the net is in a different hierarchical level than at least one other one of the blocks of the net.

17. (Original) The system of claim 12 further comprising a storage device for storing a logical representation of the hierarchical design.

18. (Original) The system of claim 12 further comprising a storage device for storing an RC model of the hierarchical design.

19. (Original) The system of claim 12 wherein a storage capacity of the external circuit analysis tool is greater than a storage capacity of the system.

20. (Currently Amended) A system for flattening a hierarchical design to be processed by an external circuit analysis tool, the system comprising:

means for reading an RC representation of the entire hierarchical design;

means for identifying a particular block of the hierarchical design to be flattened into a flat representation of the particular block, wherein the particular block is operable to include instantiations of child blocks at a level lower than the particular block's level; and

means for writing a flat representation of the particular block to an external file available to the second circuit analysis tool, wherein the instantiations of the child blocks may be rotated with respect to one another.

~~means for writing a flat representation of each block of hierarchical design to an external file.~~

21. (Original) The system of claim 20 further comprising, means responsive to flattening of all blocks of the hierarchical design for saving the external file.

22. (Original) The system of claim 20 further comprising a storage device for storing a logical representation of the hierarchical design.

23. (Original) The system of claim 20 further comprising a storage device for storing an RC model of the hierarchical design.

24. (Original) The system of claim 20 wherein a storage capacity of the external circuit analysis tool is greater than a storage capacity of the system.

25. (Original) The system of claim 20 further comprising means for saving the external file to a memory of the circuit analysis tool.

26. (Currently Amended) A computer-readable medium operable with a computer for flattening a hierarchical design to be processed by an external circuit analysis tool, the medium having stored thereon:

computer-executable instructions for reading a logical representation of the hierarchical design;

computer-executable instructions for identifying a particular block of the hierarchical design to be flattened into a flat representation of the particular block

computer-executable instructions for loading RC information for [[a]] the particular block of the hierarchical design from an RC model of the hierarchical design, the particular block including any instantiations of child blocks at a level lower than the particular block's level ; and

computer-executable instructions for writing a flat representation of the particular block to a file available ~~each instantiation of the block~~ to the external ~~second~~ circuit analysis tool, wherein the instantiations of the child blocks may be rotated with respect to one another.

27. (Currently Amended) The medium of claim 26 further having stored thereon computer-executable instructions for deleting the RC information for the particular block from the RC model subsequent to the flattening.

28. (Currently Amended) The medium of claim 26 further having stored thereon computer-executable instructions for flattening all blocks in a first hierarchical level of the hierarchical design ~~are flattened~~ before any blocks in a next hierarchical level of the hierarchical design are flattened.

29. (Original) The medium of claim 26 further having stored thereon computer-executable instructions for flatting all blocks of a net of the hierarchical design before any blocks of another net of the hierarchical design are flattened.

30. (Original) The medium of claim 29 wherein at least one of the blocks of the net is in a different hierarchical level than at least one other one of the blocks of the net.

31. (Currently Amended) A computer-readable medium operable with a computer for flattening a hierarchical design to be processed by an external circuit analysis tool, the medium having stored thereon:

computer-executable instructions for reading an RC representation of the entire hierarchical design; [[and]]

computer-executable instructions for identifying a particular block of the hierarchical design to be flattened into a flat representation of the particular block, wherein the particular block is operable to include instantiations of child blocks at a level lower than the particular block's level; and

computer-executable instructions for writing a flat representation of the particular block to an external file available to the external circuit analysis tool, wherein the instantiations of the child blocks may be rotated with respect to one another.

~~computer-executable instructions for writing a flat representation of each block of hierarchical design to an external file.~~

32. (Original) The medium of claim 31 further having stored thereon computer-executable instructions responsive to flattening of all blocks of the hierarchical design for saving the external file.

33. (Currently Amended) The medium of claim 31 further having stored thereon computer-executable instructions for saving the external file to a memory [[of]] accessible to the external circuit analysis tool.